Ultrawideband Design Challenges for Wireless Chip-to-Chip Communications and Interconnects

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Abstract— The ever growing demand for on-board space craft processing combined with the exponential advance in chip development and high pin count devices is resulting in an increased complexity in high reliability interconnect technology. When the thermal management, control of ground bounce, and power distribution issues are considered, achieving the required reliability levels for space applications with traditional interconnect technologies is becoming more of a concern. As an alternative solution, an ultrawideband (UWB) based high speed wireless method for chip to chip as well as off-board communications can be considered. Such approach would reduce the high pin count connectors and interconnects between complex components. UWB with its simple transceiver architecture, low power consumption, and high data rate within short ranges is shown to be the best candidate for the applications targeted. This paper explores the design challenges for developing a test-bed using commercial off-the-shelf (COTS) components that will be used to prove the concept of wireless chip-to-chip communications and develop associated algorithms. Energy detector based UWB transceiver is presented in this paper and our study shows the feasibility of implementation such transceiver using COTS components. The UWB transceivers will eventually be integrated into a chip eliminating the need for many of the high speed interface specific applications, and decreasing the number of the pin fields required.

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1. INTRODUCTION

Ultrawideband (UWB) is a promising technology for networks requiring a very high data rate at short distances. Chip to chip, board to board, and box to box interconnects can also make use of an UWB based wireless link. In these cases, the distances are even shorter compared to a networking application, and the UWB designer can take advantage of this fact for high speed link. The physical layer requirements for interconnects are primarily determined by the data rate needed and the tolerable bit error rate.

The current densities of devices are already approaching levels where the board designers are constantly challenged by dense layout and routing issues. The multilayer boards needed to support such devices are not only getting thicker, but complexity associated with micro vias and Plated Through Holes (PTH) are exasperating the failure rate and thermal problems. For space applications, heat dissipation is particularly a problem, since there is no conventional air

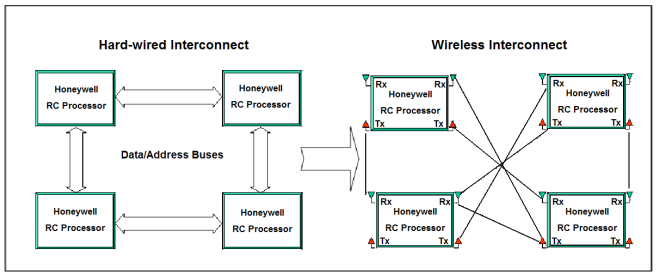

Fig. 1. Chip-to-chip wired and wireless links.

cooling available. There is also need for an alternative source of data sharing on board or between chips. The chip manufacturers have taken the route of high speed serial bus supporting multi-gigabit throughput for chip to chip communications to reduce I/O constraints. A pure wireless option or a hybrid of hardwired and wireless can provide the flexibility of reconfiguration and ease the input/output (I/O) constraints. An ideal wireless solution would be integrated into the chip, and offer option of configurability. The transceiver complexities need to be limited and accommodated into the chip fabrication. UWB offers such features, taking into account its baseband operation and fairly simple modulation and demodulation techniques.

A generic board designed for multiple applications will have to be routed as depicted in Fig. 1. Each processor, which is Field Programmable Gate Arrays (FPGAs), now has to communicate through each other if it does not have a direct trace to the device. However, a wireless link will allow the point to point communication link. Mapping new algorithms or systems that have different data rate requirements would be easily achievable with re-configuring the wireless link. With such a configurable wireless link, the data sharing and processing will allow a single device to communicate to multiple devices and vice versa. Distributed process can be easily achieved with the available bandwidth.

Determining the architecture of UWB transceiver for this application is a critical issue. Rake, transmitted-reference (TR), differential detector, and energy detector (ED) are the four most popular UWB receiver architectures investigated in the literature. To make a selection among these options, there are several aspects to be taken into account. For instance, UWB Rake receiver provides high data rate (typically up to several Gbps) but with the cost of a highly complex circuitry. On the other hand, the ED receiver architecture provides lower data rate (typically 1-100 Mbps) but with much lower complexity.

One of the factors that influence the hardware complexity in a UWB transceiver is the use of either all-digital or mixed analog-digital components. Although all-digital Rake receiver provides reconfigurability, scalability, and a high data rate it is burdensome to implement an all-digital Rake receiver with the current technology . Because high-resolution (minimum 4 bits), and large-dynamic range ADCs, as well as digital signal processing (DSP) hardware that can process tremendous amount of data within very short time [1], [2].

The RF components and digital hardware required to design a Rake receiver are expensive, and designing such components comes with some challenges. Therefore, low-complexity UWB receiver architectures such as ED and TR receivers using mixed analog-digital components are considered for the testbed design. In this paper, ED based UWB testbed design challenges along with some designed components are presented. The UWB testbed is used to prove the concept of wireless chip-to-chip communications and interconnects as well as to develop and test algorithms for fully reconfigurable architectures in spacecrafts. The architecture of the testbed will be gradually upgraded from a mixed analog and digital ED receiver to an all-digital Rake receiver.

The organization of the paper is as follows: In Section II, the proposed transceiver architecture is introduced. Section III is devoted to the comparison of different UWB pulse generation methods. In Section IV, the primary limitations of commercially available ADCs along with sampling techniques are investigated. This is followed by a study of the capabilities and limitations of current digital hardware in Section V. Radio frequency (RF) components of the testbed along with the design challenges are presented in Section VI. Section VII provides a discussion of the baseband algorithms for the testbed. Finally, the conclusions and future studies are summarized in Section VIII.

2. PROPOSED ARCHITECTURE

The proposed architecture for the implementation of UWB testbed (shown in Fig. 2 and Fig. 3) is based on the energy detector. Energy detector, which is a non-coherent detector,

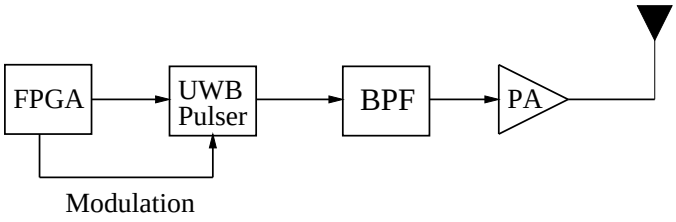

Fig. 2. Block diagram of the UWB transmitter.

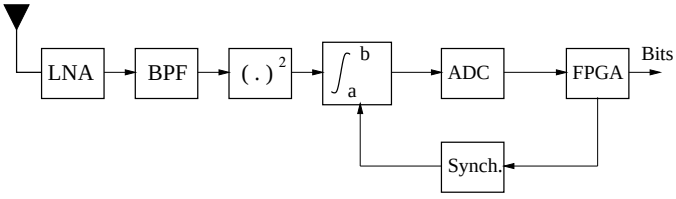

Fig. 3. Block diagram of the energy detector based UWB receiver.

requires a simple structure as well as bypasses complex channel estimation and synchronization. From the modulation options suitable for energy detectors, on-off keying (OOK) is employed.

The transmitter part of the UWB testbed consists of a Furaxa Libove UWB pulser, which is configured by an FPGAs board. The generated UWB pulses, which are modulated according to OOK, are band-pass filtered (BPF) and amplified by means of a low noise amplifier. The resulting UWB signal is transmitted via the designed UWB antenna.

In the receiver part, the UWB signal is received by another UWB antenna. Then, it is again amplified and filtered with a BPF, respectively. The demodulation of the received UWB signal is achieved by passing the signal through a square-law device (such as a Schottky diode operating in square-region) followed by an integrate-and-dump circuit and a decision mechanism, where the bit decisions are made. The output of the integrate-and-dump part is sampled by the ADC for each bit just before dumping. The samples are digitized and fed into the FPGAs, where they are compared to a predetermined threshold and a bit decision is made, accordingly. A significant issue regarding UWB reception is synchronizing with the transmitted bits. Synchronization is achieved by transmitting a training sequence, which is known by both the transmitter and receiver. By delaying the *start* and *dump* points of the integrator via the synchronization circuitry, the FPGAs device actively determines the point yielding the best match between the transmitted and received training bits. This point is then used as the synchronization point until the next training sequence is transmitted. A theoretical performance analysis is done for the proposed testbed architecture. In this analysis, the channel model in [3] is utilized, and the integration interval of the receiver is taken as $10ns$. The probability of error is plotted against E_b/N_0 in Fig. 4.

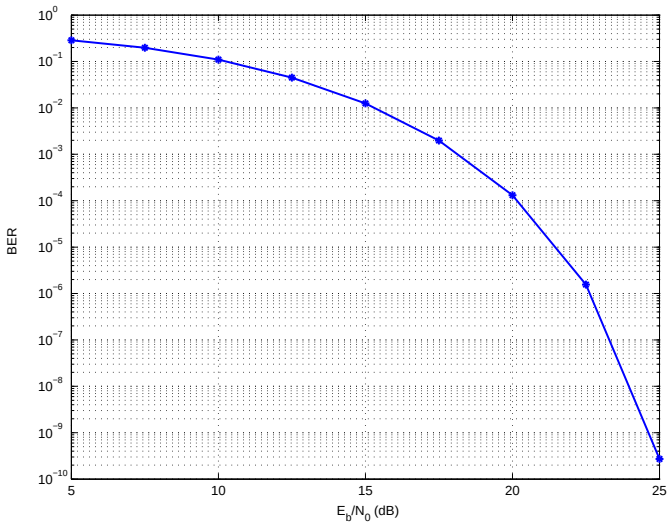

Fig. 4. Theoretical BER performance of the proposed UWB testbed

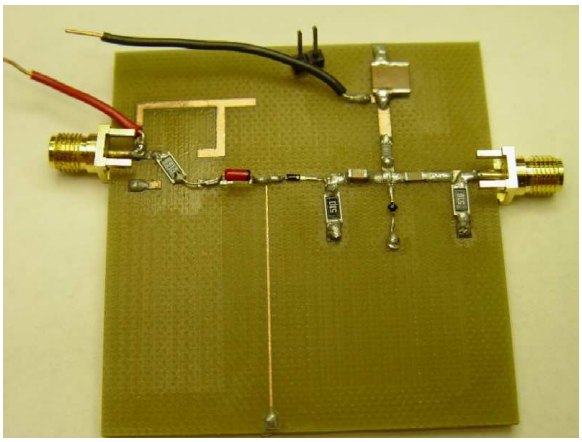

Fig. 5. Step recovery diode based UWB pulser circuit.

3. Pulse Generation Methods

One of the major design challenges for UWB transmitter is the generation of impulses on the order of 1 ns or less in width. For generating such short pulses, several techniques have been proposed. Among these techniques, the step-recovery diode (SRD) circuit and the proprietary IC pulser from Furaxa, Inc. proved to be the best candidates.

An SRD based UWB pulse generator circuit is implemented according to the design criteria in [4] and [5]. The main advantages of this circuit (shown in Fig. 5) are its simplicity and low cost. However, there are some limitations regarding this implementation. First, the pulse repetition rate is limited by the minority carrier lifetime of the device. Based on commercially available diodes, this corresponds to a maximum data rate of 200 MHz. Secondly, the diode operating point changes with temperature. This temperature instability results in jitter and noise in the circuit. A third limitation is that without additional cost and complexity it is difficult to implement a dynamic pulse generator, which has control on the pulse parameters such as pulse shape, width, and amplitude. Other problems with SRD circuits include difficulty in achieving wideband impedance matching for 50 Ω systems and the high power requirement. There are several commercially available CMOS pulse generators. One of the more affordable and flexible chip implementations of a UWB pulse generator is the Libove pulser. This system implements the UWB pulse generator in GaAs MESFET process. The result is a highly flexible pulse generator that can achieve pulse repetition rates up to 2 GHz. The control signals shaping the pulse are the *start*, *stop* and *analog input* signals. The *start* and *stop* signals control the pulse width and position of the pulse in the clock cycle, while the *analog input* signal controls the pulse amplitude.

The generated UWB pulse consists of an array of eight pulses, each 125 ps wide. By adjusting these short pulses, any desired pulse shape can be obtained. The Libove UWB pulser has some clear advantages over the step recovery diode

circuit, such as dynamic control of all pulse parameters, high pulse repetition rates, excellent temperature stability, and an integrated circuit implementation. Due to these clear superiorities, the Libove pulser is used in the UWB testbed design.

4. Analog to Digital Converters and Sampling Techniques

Analog-to-Digital Converters (ADCs) are considered critical components for the UWB testbed design due to the large bandwidth of the UWB signal. In an ADC, the analog signal is sampled and quantized depending on the sampling time and word length. The key characteristics of the ADCs considered in the UWB testbed design are the sampling rate, resolution (precision), and spurious-free dynamic range (SFDR).

In the testbed design, symbol-spaced sampling rate is considered. Therefore, the sampling rate required is 1-100 MHz, which can be achieved with commercially available ADCs. Direct and parallel time domain sampling are two commonly used sampling techniques. The incoming signal is sampled using a single ADC in the direct sampling technique, whereas in parallel time domain sampling it is sampled using multiple ADCs operating in parallel. Since the current commercially available ADCs are able to sample the incoming UWB signal at a rate of 100 MHz, the direct sampling technique is considered for the testbed design. Parallel time domain sampling is usually employed to achieve high sampling rate. This technique is suitable for all-digital rake receiver based testbed design.

It is worth mentioning the main limitations of the commercially available ADCs from UWB application perspective. One of the primary limitations of a practical ADC is the analog input bandwidth, or the range of frequencies, which the ADC can sample with very little loss in fidelity [6]. Another limitation of a practical ADC is the aperture delay variation. The aperture delay is the time delay between the rising edge of the ADC clock signal and the point where the ADC actually samples the input signal [6]. For a system utilizing a single ADC, the aperture delay is a minor concern. For the parallel time-domain sampling technique, the performance of the receiver is predicated on each ADC, which are sampling the received signal at precisely spaced intervals.

5. Digital Hardware Capabilities and Limitations

Several processors are available to process the digitized UWB signal. These processors vary substantially in architecture, speed, multiprocessor capability, physical size, dynamic range, arithmetic precision, power consumption, and cost. The processor architecture affects the efficiency of different types of algorithms that can be executed. Speed is usually a critical requirement in selecting a processor. A number of baseband component technologies can be used in the UWB testbed design. There are currently two major approaches regarding these technologies. The first approach consists of the traditional integrated circuit (IC) computing technologies, which are based on mapping the algorithm to a fixed set of hardware resources/requirements. There are five main baseband component technologies in this category: Microprocessor (uP), Digital Signal Processor (DSP), Field Programmable Gate Arrays (FPGAs), Application-Specific Integrated Circuits (ASIC), and Heterogeneous Processing Systems. The second approach is the adaptive computing technologies, which are based on mapping the hardware to the algorithm requirements. In other words, both the algorithm and hardware resources are dynamic. The Adaptive Computing Machine (ACM) from Quicksilver Technology and the PicoArray from Picochip Corporation are two sample technologies in this category. For example, at 200 GOPS (giga operations per second) and 40 GMACs (Giga MACs), the PicoArray is one of the most powerful signal processors available, delivering ten-times the price performance of the traditional DSP or FPGAs [7]. Since the technologies under the second category have less mature design tools and are more expensive than DSP processors and FPGAs, these

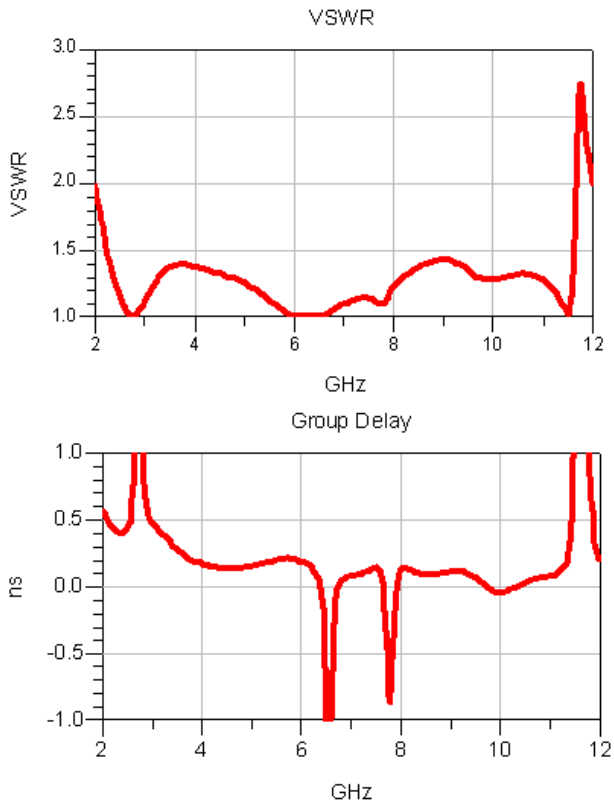

Fig. 6. Simulated VSWR and group delay data for the coplanar waveguide monopole antenna.

technologies are not considered for the UWB testbed design. We will discuss only the DSP processors and FPGAs in this paper.

DSP processors have a fixed processing architecture and the capability to execute different algorithms based on a sequence of instructions typically stored in the memory. Although DSP processors have a high-function capability, their performance is very low. Since UWB algorithms require high-performance processors, current DSP processors within a reasonable price range are not suitable for the UWB testbed design. On the other hand, programmable logic devices have been available for many years, but it is only recently that FPGAs have become so powerful that they have begun to displace the ASICs and DSPs in the leading-edge digital transceiver design. The FPGAs approach to signal processing provides a high-performance, highly flexible, miniature silicon foundry at the desired disposal, with a turn-around time of hours instead of months or even years required for many complex ASICs. New FPGAs devices utilize extremely small silicon geometries allowing both very high clock speeds and low core voltages [8]. For example, the Xilinx Virtex-II Pro XC2VP70 contains up to 996 high-speed I/O pins, 328 hardware multipliers, up to two 400 MHz PowerPC processor cores, and was designed especially for processing large amounts of data at very high rates. This is evident by the Virtex II Pro implementation of double-data rate (DDR) registers. These registers store data on the rising and falling edge of the clock, which allows for the FPGA clock to be run at 250 MHz to input 500 MHz data [9]. The FPGA is promising to be most suitable current technology for UWB testbed design. Virtex-II XtremeDSP development kits from Nallatech corporation is used in the testbed design. This board contains Xilinx virtex-II (XC2V3000-4FG676) device with two independent ADC (14-bits up to 65 MSPS) and DAC (14-bits up to 160 MSPS) channels.

Fig. 7. UWB antenna designed and fabricated for the testbed.

6. RF COMPONENTS

In UWB impulse radio systems, the RF front-end design must be optimized to minimize signal distortion. The performance of the antenna, low noise amplifier (LNA), and band pass filter (BPF) directly affect the ability to transmit and receive sub-nanosecond pulses. UWB antennas receive all frequencies across the entire bandwidth at the same time, therefore the phase center, gain, group delay, spectral pattern, and voltage standing wave ratio (VSWR) must be nearly fixed. The UWB antenna pass-band should have linear phase with no resonant frequencies to avoid group delay spikes. Antennas with variable gain within its radiation characteristics can cause pulse distortion to occur at different angles of arrival to the receiver antenna. The ringing effect can be a problem in UWB antennas. Once the antenna receives a pulse, it can oscillate and slowly dampen in time, obliterating the impulse characteristics of the signal. Resistive antennas with low Q can be used to avoid this problem. UWB antennas are pulse-shaping filters [10]. Any distortion caused by the antenna in the frequency domain will cause distortion of the transmitted pulse shape. The UWB RF front-end designer must be aware that pulse shaping is indeed related to the design of the antenna and hence both should be considered as a whole.

Two 2”x2” omni-directional UWB antennas (shown in Fig. 7) fabricated on FR4 31 mil substrates for the UWB testbed took all these conditions into account. In the future, the antennas will be designed on a low loss substrate (i.e. Rogers RO4350B) with better dielectric constant uniformity in order to improve radiation efficiency and maximize product yield. The antennas are single-feed coplanar monopole antennas with linear polarization. Circular polarization has not been studied here but may be created by adjusting the feed to a position where two near-degenerate orthogonal modes with equal amplitudes are created at the mean fundamental frequency. Tuning can be performed by adjusting the curvature of the ground plane edges as well as the radius of the semi-circle of the monopole. The EM simulated VSWR and group delay data for these antennas are plotted Fig. 6. Note that the VSWR for this antenna design is well matched, but may cause signal distortion if used up to 10.6 GHz due to the group delay spikes occurring between 6 and 8 GHz.

When choosing a UWB LNA, bandwidth, gain, group delay, power consumption, dynamic range, impedance matching, linearity, and noise figure are important parameters to consider. An LNA gain-bandwidth product typically determines its suitability for use in UWB systems. UWB LNAs must provide adequate and nearly constant gain and group delay over the entire bandwidth. Noise figure and linearity requirements are not as important as other parameters due to the

large available bandwidth. An LNA dynamic range of 40 dB is typically required in UWB systems; however, narrow band interference (NBI) can be 60 dB above UWB signals and must be considered. Using notch filtering to avoid NBI may help avoid this problem allowing lower dynamic range LNAs to be utilized.

A UWB BPF design operating from 3.1 to 10.6 GHz can be created using an edge-coupled microstrip filter design. However, due to the large bandwidth, the BPF resonators require very tight coupling (<3 mil). These types of tolerances require precise manufacturing abilities and hence are expensive. In [11], a ring resonator BPF with open stubs is presented. Fig. 8 shows a modified version of this filter with shorted stubs (to improve low frequency performance) and a series low-pass filter (to improve the high frequency performance). This BPF prototype was fabricated on 20 mil Rogers 4350 substrate material. In Fig. 9, the s-parameters for this BPF are demonstrated. This type of filter is less susceptible to manufacturing tolerances when compared to an edge-coupled filter that requires 3 mil spacing between its resonators. When designing a BPF, the RF designer should pay attention to minimizing the order of the filter because it is directly proportional to the group delay. In fact, the group delay shows spikes and increases at the cutoff frequencies of a BPF as the skirts of the filter become steeper. The designer should also aspire to make the pass band as flat as possible while minimizing the insertion loss.

7. UWB Baseband Algorithms

Synchronization

UWB transmission necessitates a rapid and accurate synchronization algorithm. The algorithm is required to process large amounts of data (number of possible synchronization points) within non-prohibitive time, and it must be able to estimate the time offsets accurately due to the very short pulses being used. UWB synchronization consists of initial acquisition of the signal, code tracking, and a control logic that manages the transition between acquisition and tracking modes. The key parameter for acquisition algorithms is the mean acquisition time, which is a function of probability of detection, probability of false alarm, number of possible synchronization points, and the length of the PN sequences [12]. The acquisition has four levels: symbol-level, frame-level, pulse-level, and multipath-level acquisition. Depending on the receiver architecture, some of the acquisition levels may not be required. For example, if a rake receiver is employed, all four-acquisition levels need to be performed. On the other hand, for an ED based architecture, there is no need to estimate the time offsets of each path. Therefore, an ED relaxes the synchronization process by reducing the processing time and the required DSP power.

Since ED based testbed design is considered, only symbol-, frame-level acquisitions along with the adaptive synchronization algorithm (see Section II) are performed. In the symbol-level acquisition, the receiver checks whether the incoming signal exists or not. If it exists, then the received signal is correlated with the locally generated PN code during frame-level acquisition. Each possible code phase is evaluated in this level, and the phase that results in maximum correlator output is selected as the correct PN code.

Although adaptive threshold and integration interval estimation algorithms improve the BER performance of the ED based testbed, fixed threshold and integration interval are considered initially. A serial search scheme is also employed due to its simplicity even though faster search algorithms exist. Once the initial signal parameters are acquired, the next step is to track the signal. Although the time offsets and the code phase of the signal are estimated, the signal arrival time may drift over time due to discrepancy of the

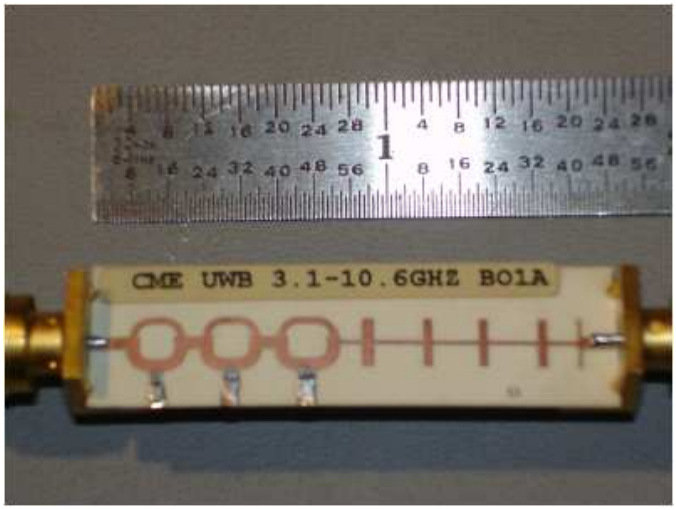

Fig. 8. Band-pass filter specifically fabricated for the UWB testbed.

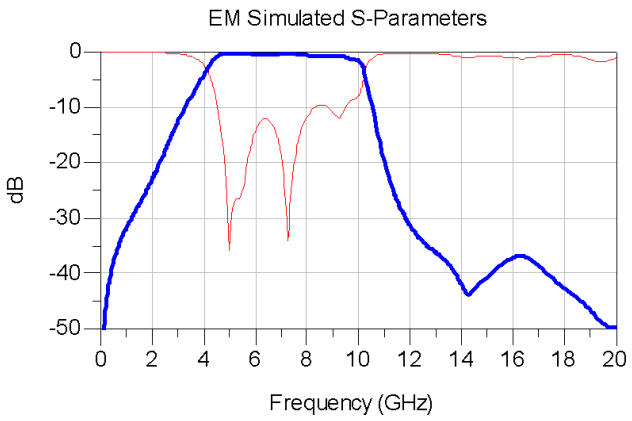

Fig. 9. EM Simulated data of shorted stub ring resonator with low pass filter. Legend: Red/thin line = s11 data, blue/thick line = s21 data.

transmitter and receiver clock frequencies, and the channel behavior. The initial estimated arrival time may not be correct anymore. Therefore, a code-tracking algorithm is needed to track the drifting signal. One of the most commonly used code tracking algorithms is the early-late tracking algorithm. The transition between the initial signal acquisition and code tracking modes is handled by control logic circuit. The synchronization algorithm can be implemented in the FPGAs.

Detection

A simple detection algorithm with a fixed threshold is employed. If the amplitude of the incoming signal is above the threshold the estimated bit is detected as 1, otherwise as 0. The detection algorithm can also be implemented in the FPGAs. The samples at the output of ADC are processed by the FPGAs, and each sample is compared to the predefined threshold. The threshold is a function of the expected pulse amplitude and variance of the noise. Noise level can cause the decision device to make incorrect bit decisions, which result in high bit error rate. After determining the threshold, the received data is processed according to the modulation technique.

8. Conclusions and Further Research

The primary capabilities and limitations of commercially available testbed components such as ADCs, digital hardware including DSP and FPGAs, and LNAs are investigated. The bandpass filter and antenna designed for the testbed are presented. The implementation of synchronization and detection algorithms in FPGAs are discussed. The investigations show that the energy detector based UWB testbed is feasible to be implemented using the commercially available mixed analog and digital components. Aiming at a UWB transceiver that can be employed in chip to chip communications in space applications, further efforts will be given to upgrade the current testbed from mixed analog-digital energy detector toward the all-digital ED as well as Rake receiver based testbed.

9. Acknowledgements

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Biographies

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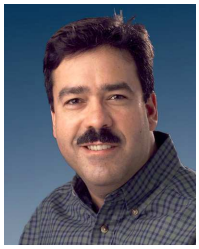
Jamal Haque is a Principal Systems Engineer at Honeywell, Clearwater, FL. He has worked for AT&T Paradyne, Rockwell Semiconductor and Lucent Technology (Bell Labs) developing algorithms for wireline and wireless physical layer design. At Bell labs he was a integral part of Sirius Satellite Radio receiver design team. Current research interests include advance modulation scheme for high speed data networks and spaceborne wireless inter-connectivity for reconfigurable systems. He holds eight patents in various technique's in data communications and signal processing system. He graduated from University of South Florida(USF), Tampa, FL with BSEE(1990) and MSEE(1993), specializing in communication system and signal processing.



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David P. Markell received his B. S. and M.S. degrees in electrical engineering on Dec. 1998 and Dec. 2004 respectively at the University of South Florida (USF), Tampa, FL. From 1999 to 2004 he was an integral member at Modelithics, Inc. creating microwave active and passive component models. Presently, he is employed by Custom Manufacturing & Engineering (CME) in St. Petersburg, FL working on remote sensing radiometers, ad-hoc wireless network design, and UWB radar and transceiver design. Current research interests include smart antenna design for ad-hoc wireless sensor networks, cognitive radio design, and microwave remote sensing.