A Channelized DSSS Ultra-Wideband Receiver

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ABSTRACT

Critical to the design of a digital ultra-wideband (UWB) receiver is the ability for the analog-to-digital converter (ADC) to efficiently sample and digitize the UWB signal of several gigahertz. Designing a single ADC to operate at such frequencies is impractical, and parallel ADC architectures with each ADC operating at a fraction of the effective sampling frequency need to be devised. A parallel receiver architecture that efficiently samples and processes the UWB signal at a fraction of the chip frequency is proposed. The received signal is channelized in the frequency domain by employing a bank of mixers and lowpass filters. After sampling at a much reduced frequency, digital filters then operate directly on the sampled signals in each subband channel to optimally estimate multiple spread codes in parallel.

1. INTRODUCTION

The ultra-wideband (UWB) radio operates by spreading the energy of the radio signal very thinly from near d.c. to a few gigahertz. Since this frequency range is highly populated, the UWB radio must contend with a variety of interfering signals, and it must not interfere with narrowband radio systems operating in dedicated bands. These requirements necessiate the use of spread-spectrum techniques. Both time-hoping spread spectrum (referred to as impulse radio) and direct-sequence spread spectrum (DSSS) UWB systems have been studied [1]. This paper focuses on DSSS UWB systems, although the reception techniques described in this paper are equally applicable to impulse radios.

In an UWB receiver, the analog-to-digital converter (ADC) can be moved almost up to the antenna as shown in figure 1. Critical to this design approach, however, is the ability for the ADC to efficiently sample and digitize at least at the signal Nyquist rate of several gigahertz. Designing a single ADC to operate at such frequencies is impractical, and parallel ADC architectures with each ADC operating at a fraction of the effective sampling frequency need to be devised. In addition, the ADC must support a very large dynamic range to resolve the signal from the strong narrowband interferers. Even if such high performance ADC is available, the digital circuitries need to process the received signals at prohibitively high clock frequencies. The receiver, therefore, must perform the digital signal processing at a fraction of the effective sampling frequency.

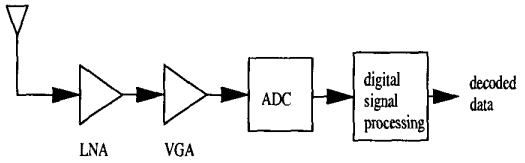

Figure 1 : UWB receiver architecture.

To overcome these practical problems, we propose a parallel receiver architecture that efficiently samples and processes the UWB signal at a fraction of the chip frequency. This architecture achieves high reception performance in the presence of strong narrowband interferers and enjoys numerous implementation advantages as described in subsequent sections.

2. RECEIVER ARCHITECTURE

To sample at a fraction of the chip frequency, the received analog signal needs to be channelized either in the time or frequency domain. An approach that has been used in high-speed digital sampling oscilloscopes is to employ an array of M ADC's each triggered successively at $1/M$ the effective sample rate of the parallel ADC [2]. A fundamental problem with an actual implementation of such time-interleaved architecture is that each ADC sees the full bandwidth of the input signal. This causes great difficulty in the design of the sample/hold circuitry because of its high sensitivity to clock jitter. In addition, in the presence of strong narrowband interferers, each ADC requires an impractically large dynamic range to resolve the signal from the narrowband interferers.

Instead of channelizing by time-interleaving, the received signal can be channelized into multiple frequency subbands using a bank of bandpass filters and an ADC in each subband channel operating at a fraction of the effective sampling frequency [3]. An important advantage of channelizing the UWB signal in the frequency domain is that the dynamic range requirement of each ADC is relaxed, since the frequency channelization

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process isolates the effects of a large narrowband interferer. The sample/hold circuitry in the subband ADC, however, is still very difficult to design as it sees the entire signal bandwidth at the high-frequency subbands. In addition, sharp bandpass filters with high center frequencies, which are necessary to mitigate the effects of strong narrowband interferers, are extremely difficult to realize especially in integrated circuits.

2.1 Analog section of the proposed receiver

Because of the advantages of channelizing in the frequency domain, the proposed architecture is based on the subband ADC architecture. Instead of using bandpass filters with high center frequencies, channelization can be achieved using a bank of M mixers operating at equally spaced frequencies and M lowpass filters to decompose the analog input signal into M subbands. In addition to obviating the need to design high frequency bandpass filters, channelizing the received signal using this approach greatly relaxes the design requirements of the sample/hold circuitry. The sample/hold circuitry in this architecture sees only the bandwidth of the subband signal; whereas in the bandpass channelization approach, the sample/hold circuitry sees the entire signal bandwidth at the high-frequency subbands. Consequently, the required sampling aperture, which is the amount of time required for the sampler to capture the input value, is much more relaxed in the proposed channelization approach.

A specific example of the proposed architecture with three subband channels (i.e., $M = 3$) is shown in figure 2. It employs a bank of complex mixers operating at equally spaced frequencies (denoted as f_1 and f_2) and lowpass filters (denoted as $H(j\Omega)$) to decompose the analog input signal into three subbands. The lowpass filter $H(j\Omega)$ are designed to have sharp rolloffs with large attenuation in the stopband frequency to achieve greater robustness to strong narrowband interferers as described in subsequent sections. In figure 2, the zeroth subband signal (denoted as $s_0(t)$) is a real signal as no downconversion is performed, and the remaining subband signals (denoted as $s_1(t)$ and $s_2(t)$) are complex signals. Thus, to achieve the effective sampling frequency of f_{eff}, the proposed channelizer requires a total of $2M$-1 ADC's each operating at $f_{eff}/(2M\text{-}1)$. The mixer frequencies are chosen to be multiples of each other (i.e., $f_i = if_1$, $i = 1, 2, ..., M\text{-}1$), because a simple frequency divider can then be used to generate the multiple frequencies. Sampling in each ADC occurs at f_{chip}/γ, where f_{chip} is the chip frequency and γ is an integer value. In the example in figure 2, $\gamma = 2$.

2.2 Digital section of the proposed receiver

The sampled signals in each subband channels are then modulated as shown in figure 2. The purpose of the modulator is to make the channel response time invariant and the additive noise wide-sense stationary (WSS). This is described in greater detail in [4].

Instead of first reconstructing the received signal, the proposed architecture operates directly on the sampled signals to estimate the spread code as shown in figure 2. This is achieved by filtering each subband channel to estimate the γ spread codes in parallel (since chip frequency is γ times the sampling frequency) before despreading. The filter outputs corresponding to the non-zero subband channels are converted to a real signal before summing. This is necessary since the transmitted spread code is real.

An important implementation advantage for the digital section of the proposed architecture is that all of the receiver functions are performed at the sampling frequency, which is at a fraction of the effective sampling frequency. Performing the receiver functions at this reduced frequency compared to a conventional receiver, which operates at the effective sampling frequency, greatly relaxes the digital circuitries and allows the use of well-known low-power techniques.

3. SYSTEM MODEL AND FILTER DESIGN

The digital filters in the proposed architecture perform matched filtering, noise whitening, and equalization to estimate the spread code directly based on the sampled signals. To design such filters and to quantify the resulting receiver performance, we view the channelizer as a diversity communication receiver with each subband channel corresponding to a diversity communication channel. This perspective allows the use of well-known techniques to design digital filters that optimally estimate the transmitted signal in the minimum mean-square-error (MSE) sense.

An overall system model is shown in figure 3. The ith incoming bit stream $b[i]$, where $b[i] \in \{1, -1\}$ and assumed constant for N chip periods, is spread by the pseudo-random (PN) code $c[i]$, where $c[i] \in \{1, -1\}$. The resulting spread code, $x[i]$, is scaled by the magnitude of the transmit filter $\|p\|$ at a rate of f_{chip}, then passed through a normalized transmit filter $\varphi_{tr}(t)$. The resulting transmit power is $\|p\|^2$. The transmit signal $x(t)$ is then filtered by the transmit and receive antennas, whose impulse responses are denoted as $a_{tr}(t)$ and $a_r(t)$, respectively. The resulting signal is corrupted by $n(t)$, which is an additve white Gaussian noise (AWGN) of two-sided noise power spectral density equal to $N_0/2$,

and a narrowband interferer $I(t)$. The corrupted signal is then passed through an anti-alias filter, $\varphi_{\text{alias}}(t)$,which is assumed to be an ideal lowpass filter with a gain transfer of $\sqrt{1/f_{eff}}$ over the frequency range of $-\pi f_{eff} \le \Omega \le \pi f_{eff}$. For comparison purposes, the resulting signal, $y(t)$, is the input to both an ideal conventional receiver, which samples at f_{eff}, and the proposed receiver. Although the anti-alias filter is not needed in the proposed receiver, it is employed so that a fair comparison can be made between the two receivers.

The transmit filter $\varphi_{tr}(t)$ is modeled as a Gaussian pulse with a standard deviation of σ, so that the pulse is differentiable when passing through the antennas, which are modeled as differentiators. This simplified model has been shown experimentally to be reasonably accurate for Gaussian pulses and have been used to analyze impulse radios.

The output signal for the kth subband channel just before the sampling device can be written as

$$s_k(t) = \sum_i x[i] e^{-j\Omega_k t} p_k(t - iT_{chip}) + n_p(t) e^{-j\Omega_k t} \otimes h(t) \quad (1)$$

where $\otimes$ denotes convolution, T_{chip} is the code chip period, $p_k(t) = \|p\| \varphi''_{tr}(t) \otimes \varphi_{alias}(t) \otimes e^{j\Omega_k t} h(t)$, $\varphi''_{tr}(t)$ is the 2nd derivative of normalized transmit filter $\varphi_{tr}(t)$, $\Omega_k = 2\pi f_k$, $h(t)$ is the impulse response of $H(j\Omega)$, and $n_p(t) = (n(t) + I(t)) \otimes \varphi_{alias}(t)$.

Sampling at time instant $t = lT_{sample} = \gamma l T_{chip}$, where T_{sample} is the ADC sampling period, and γ and l are both integers, the resulting signal after digitally modulating is

$$y_k(\gamma l T_{chip}) = \sum_m x[m] p_k((\gamma l - m) T_{chip}) e^{j\Omega_k \gamma l T_{chip}} + e^{j\Omega_k \gamma l T_{chip}} \left(n_p(t) e^{-j\Omega_k t} \otimes h(t) \Big|_{t = \gamma l T_{chip}} \right) + n_{q_k}[l] \quad (2)$$

where $n_{q_k}[l]$ is the ADC quantization noise of the lth sample in the kth subband channel.

The signal given in (2) can be viewed as corresponding to the samples in the kth receiver among M parallel receivers. The first term on the right hand side of (2) represent the inter-chip interference and the remaining two terms represent the additive colored noise. Based on this model, digital filters that minimize the MSE can be readily computed using known optimization techniques [4]. Since γ spread codes are estimated at every clock cycle, the unbiased signal-to-noise ratio (SNR) is the average unbiased SNR of the γ spread code estimates.

4. RESULTS AND DISCUSSION

The average unbiased SNR is compared against the ideal conventional receiver, which is defined as a receiver that samples at f_{eff} (shown in figure 3) then employs an infinite length fractionally spaced linear filter to estimate the spread code before correlating. As a reference for comparison, we employ the matched filter bound (MFB) when no narrowband interference is present. This bound is given by

$$SNR_{\text{bound}} = \frac{\|p\|^2}{N_0/2} \quad (3)$$

Throughout this section, the following assumptions are made: $M = 5$; $f_{sample} = f_{chip}/3$; $f_i = i \cdot f_{sample}$, where $i \in \{1, 2, 3, 4\}$; $H(j\Omega)$ is a Butterworth filter with cutoff frequency of $f_{sample}/2$; $f_{chip} = 0.35\sigma$, where σ is the standard deviation of Gaussian transmit pulse; $f_{eff} = 3f_{chip}$; $I(t)$ is a real brickwall narrowband interferer with center frequency I_f, magnitude I_{mag} greater than $N_0/2$, and bandwidth of $0.15f_{chip}$.

Figure 4 plots the spread SNR against N_f with and without a narrowband interferer present when SNR_{bound} = -10dB assuming infinite resolution ADC's. The center frequencies of the narrowband interferer, I_f, are $0.225f_{chip}$, $0.525f_{chip}$, and $0.825f_{chip}$ each with I_{mag} = 60dB. When no interference is present, less than ten taps are required to achieve near optimal receiver performance. In the presence of a narrowband interferer, however, near optimal receiver performance is achieved for N_f of approximately 30 taps. These additional filter taps are required to suppress the effects of the narrowband interferer.

Since frequency channelization isolates the effects of the narrowband interferer, the proposed receiver achieves greater robustness to a narrowband interferer when sharper channelization filters are employed. This effect is illustrated in figure 5, which is a plot of the spread SNR versus the filter order of $H(j\Omega)$. The assumptions in this figure are SNR_{bound} = -10dB, I_{mag} = 50dB, $I_{mag} = 0.675f_{chip}$, and $N_f = 30$. If infinite bit resolution is available, the filter order does not affect the receiver performance. However, when there is only a finite number of bits in the ADC, sharper filters better isolate the increase in the quantization noise power due to the narrowband interferer. In figure 5, the performance of the proposed receiver improves steadily compared to the ideal conventional receiver as the filter order increases. This improvement saturates when the filter order is approximately four for $b = 7$ and eight for $b = 4$, which correspond to performance improvements of roughly 3dB and 20dB, respectively, compared to the

ideal conventional receiver. Thus, significant performance improvements are possible by increasing the filter order, especially when the available ADC resolution is low.

Acknowledgements

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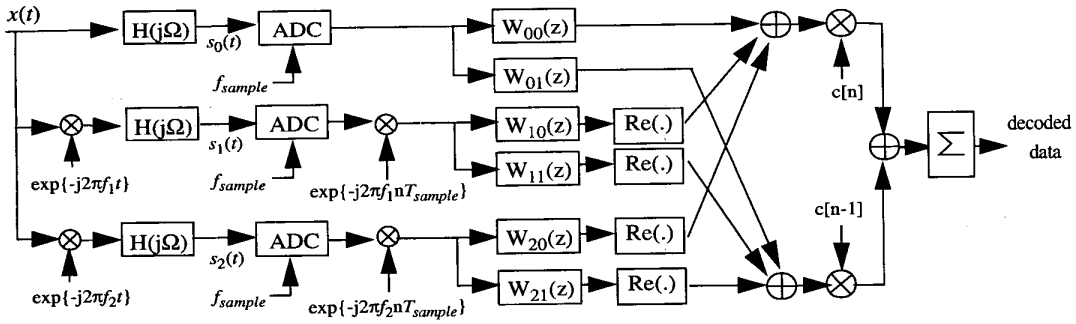

Figure 2 : Proposed receiver architecture with three channels.

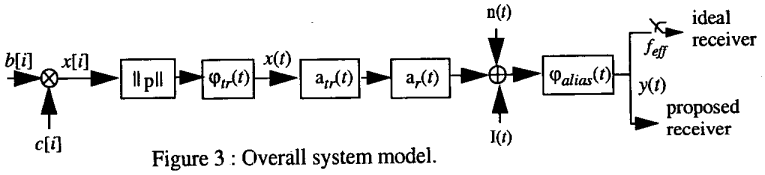

Figure 3 : Overall system model.

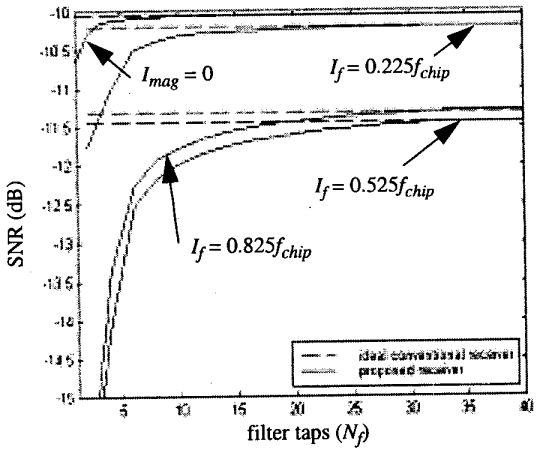

Figure 4 : SNR vs. filter taps (N_f) with I_{mag} = 60dB.

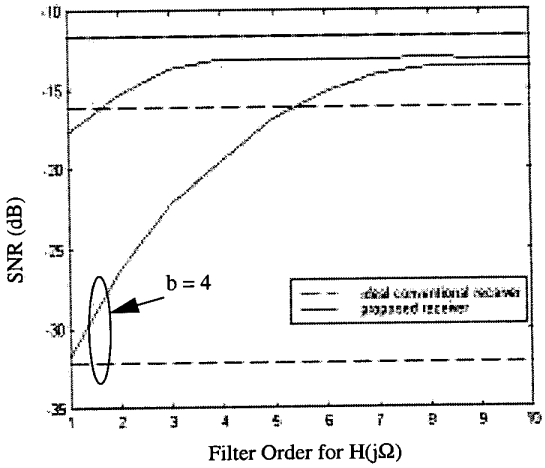

Figure 5 : SNR vs. filter order for I_{mag} = 50dB.