Low Power CMOS Re-programmable Pulse Generator for UWB Systems

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Abstract: In this paper we discuss the design of a CMOS based pulse generator for impulse-based UWB systems. The basic structure of our design involves a power amplifier with four control taps, which essentially decides the shape of the generated pulse. The design is versatile and may be used in a variety of UWB modulation schemes and systems. In addition, this design can also be incorporated into a multiband approach as a rectified cosine generator.

I. Introduction

Currently, two different approaches are widely considered for UWB systems, an OFDM based multi-band approach and an impulse-based single/dual band approach. Implimenting an impulse-based radio allows for a simpler circuit structure with less power dissipation than a multi-band approach since there is no need to up-convert a carrier signal. Also, a UWB impulse radio can potentially use a bandwidth of over 7GHz, reducing the chance of fading in a frequency slective channel, resulting in better immunity to destructive channel environments.

Many existing UWB pulse generators are based on approaches developed for radar applications and involve techniques similar to those in a Marx bank generator, capable of implementing only a single type of pulse [1]. One similar technique involves the use of a MESFET, step-recovery diode, Schottky diode, transmissions lines, and an amplifier to generate monocycle pulses [2]. Existing UWB chips have been realized in silicon germanium (SiGe) technology, such chips are estimated to cost between $20 and $30[3]. Implementing an impulse-based UWB radio in CMOS would have a much lower cost than a SiGe solution, making it more appealing for an application such as RFID. RFID technologies cover a wide array of low data rate applications that require low power and low cost. Applications of RFID include inventory control, employee identification, access control, and many others.

SiGe is used mainly because it is able to directly support high frequencies without very much difficulty. In order to use CMOS technology to generate sub-nanosecond pulses, the high frequency requirements of the system must be reduced and techniques must be employed which relax the specifications to frequencies at which CMOS technology can operate.

We present a design for a CMOS based pulse generator that is capable of generating various shaped pulses. Our design is highly versatile and can be extended to various applications with a few simple modifications. In this paper, we present our Gaussian monocycle pulse generator that is capable of meeting the FCC's spectrum regulations in the band from 3.1 to 10.6 GHz.

II. Basic Structure

The basic structure of our design involves a power amplifier with four control taps, A through D, as shown in Figure 1. The desired pulse to be generated is broken up into specific transitions in

time. The pulse generator generates the desired pulse through a combination of specific input transitions on the control taps.

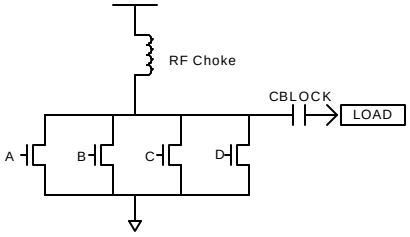


Figure 1: The Structure of a Basic Pulse Generator

In Figure 1, suppose that the control taps A, B, C, and D are set to GND, Vdd, Vdd, and GND, respectively. The power amplifier is in an idle state with no current flowing to the load. Note that the current flows through the RF choke and the two conducting transistors. We illustrate the generation of a positive Gaussian monocycle pulse as an example. From the idle state, suppose that the control tap B switches to 0 volt, turning the transistor B off. The current flowing through the transistor B starts to flow through the capacitor to the load, generating a positive slope of a pulse. After a certain delay, the control taps A and D are turned on. Then the current starts to flow in the opposite direction, generating the negative slope of the pulse. Lastly, the control tap C is turned off, and the direction of the current changes again, generating a positive slope of the pulse. Figure 2 shows a waveform illustrating the switching sequence of the four control taps and a resultant Gaussian monocycle pulse.

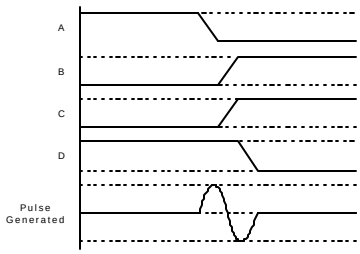


Figure 2: Pulse Generation Example

In addition to generating a positive monocycle pulse as described above, this four-tap power amplifier can also generate both positive and negative Gaussian pulses and monocycle pulses through different input switching sequences.

Figure 3 presents a partial transition diagram and the shape of the generated pulses from an initial state. The "Positive" or "Negative" of a state denotes the starting slope of the pulse generated, and the four binary values are the final values of the four control inputs, A, B, C, and D, respectively. The order and timing of the control inputs determine the shape of pulses generated as shown in Figure 3. The label associated with a transition indicates the order of the inputs that is necessary in to change from the initial state 0110 to the final state 1001, and commas indicate the delays between two input changes. For example, if the control input A changes to 1 first, followed by the simultaneous change of B and C, and then by a change of D, this is labeled as "A,BC,D". This example results in the generation of a negative pulse, as shown in Figure 3. The diagram suggests that the introduction of more control taps combined with variations of the timing and the order of control inputs enables us to generate various shapes of pulses such as Gaussian doublets.

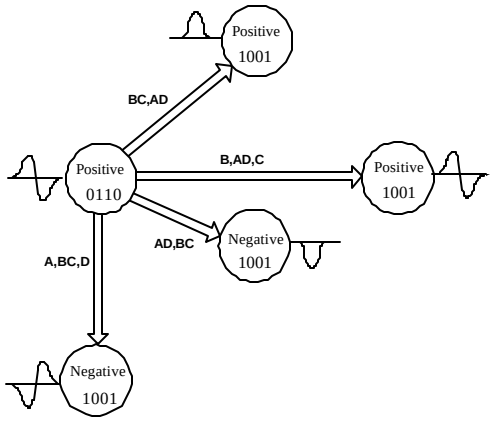


Figure 3: Control Tap State Transition Diagram

III. Pulse Generator Design

We designed our pulse generator with the target technology of the TSMC 0.18 μm CMOS processing under the supply voltage of 1.8 V. The number of taps, i.e., transistors, in Figure 2 determines the fidelity of the pulse shape generated, and the size of the transistors mainly determines the amplitude of the pulse. In order to minimize power consumption, control logic complexity, and area, we chose a four-tap power

amplifier capable of generating pulses with constant amplitude.

In order to support the timing requirements and the desired modulation scheme, a control logic block consisting of a state machine, delay elements, and a set of D FFs was developed. Figure 4 shows the entire block diagram of our pulse generator including a bandpass filter. The bandpass filter is added at the output of the pulse generator to remove any DC offset and to eliminate the out-of-band, undesired, spectrum. The delay generator block delays the clock signal by a certain amount of time, and the delayed clock signals are used to control the timing of the control inputs. The necessary delay for each stage of the delay generator was obtained through simulation and is set to 50 ps for our design.

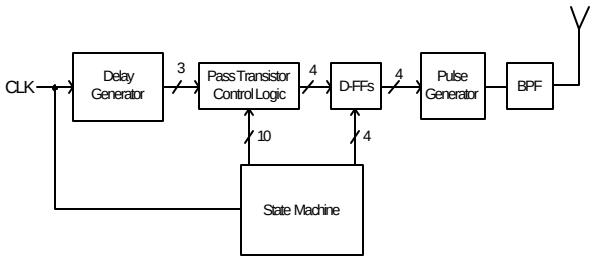
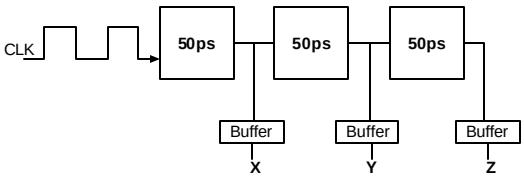


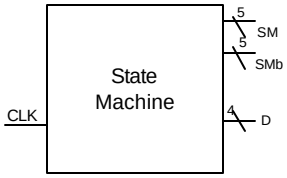
Figure 4: A Block Diagram of Pulse Generator

Figure 5 shows a more detailed view of the control logic. The delay generator produces the necessary delayed clocks, and the state machine generates the timing signals that signal the D FFs to generate the control signals in the appropriate order. The delayed clock signals trigger the four flip-flops at appropriate times controlled by the state machine, and the FF outputs generate the necessary switching at the inputs of the four taps of the power amplifier.

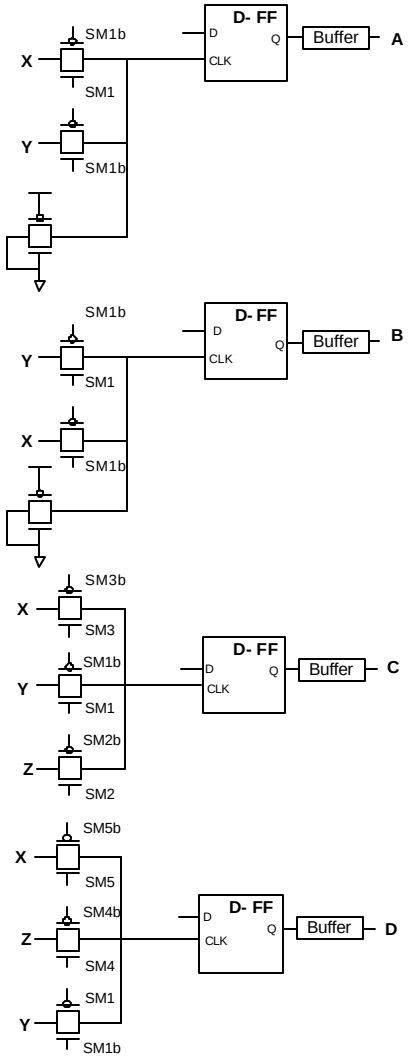
A critical part of the design is to develop the 50 ps delay elements, which are essential to the shape of the pulses generated. MCML (MOS Current Mode Logic) circuits, which are faster than other logic families at the cost of larger power consumption, are used to generate the delays. Each delay element consists of 2 MCML inverters and a buffer. Shown in Figure 6 is an MCML



(a) Delay Generation



(b) State Machine



(c) D FFs and Associated Logic

Figure 5: Control Logic Block Diagram

inverter/buffer circuit; note that the same circuit is used for an inverter or a buffer. Three of these circuits were cascaded to form the 50ps delay element. The bias voltage for RFP and RFN are set to 0 and 1.8 volts, respectively. The two P-transistors at the top of the circuit act as resistors and the N-transistor at the bottom acts as a current source. As the values of the inputs change, the current swing from one side to the other, raising and lowering voltage levels on the two outputs accordingly.

Like any MCML circuits, the MCML inverter/buffer requires complimentary and non-complimentary input pairs. After simulating the timing requirements for the delay between the differential inputs, we found that a small time delay between them has little impact on the overall performance of the MCML delay element. Hence, a simple CMOS inverter is used in our design to generate a complimentary input.

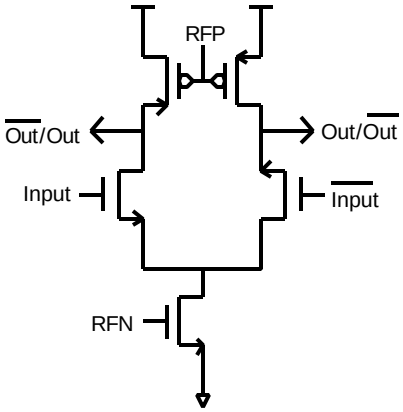


Figure 6: A MCML Inverter/Buffer

Three MCML delay elements, each with a 50 ps delay, were cascaded to form a 150 ps delay element, with three outputs, 50 ps, 100 ps, and 150 ps delays, as shown in Figure 5 (a). Since the delay of an MCML circuit is directly proportional to the load that is applied [4], through simulations the transistors were sized to meet our 50 ps delay requirement. In order to maintain a delay of 50ps between each delay element, the transistors were sized such that the first delay element is approximately 3 times the size of the last delay element and the second delay element is twice the size of the last.

Power Saving

The four-tap power amplifier has two active transistors in the steady state, consuming a large amount of power due to their large size. In addition, the bias current for MCML circuits also contributes a large amount of static power dissipation.

To reduce the overall power consumption, we developed a power saving scheme that can significantly reduce the overall power consumption for low data applications such as RFIDs. The basic scheme involves turning on the pulse generator, generating a desired pulse (in 3 clock cycles), and turning the generator off. It can easily be achieved through the state machine by setting all the inputs of the D flip-flops to 0 volts, thereby turning off the 4 transistors in the power amplifier on the next clock pulse. The MCML delay circuit can also be turned off by changing the bias voltage of RFN to 0 volt.

As an example, Figure 7 illustrates the timing of our pulse generator for a data rate of 500 bps with a clock frequency of 250 MHz, which is sufficient for most RFID applications. The pulse generator turns on for 12 ns to send one significant bit accompanied by two spurious bits and consumes 57.15 mW during the time. Then, it is turned off for about 20 ms, (precisely speaking, 19,999,988 ns) consuming only 8.44 µW during this period. So the average power consumption is reduced to 8.47 µW owing to the power saving scheme.

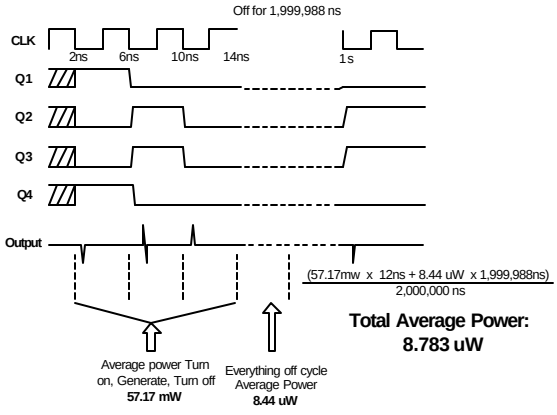
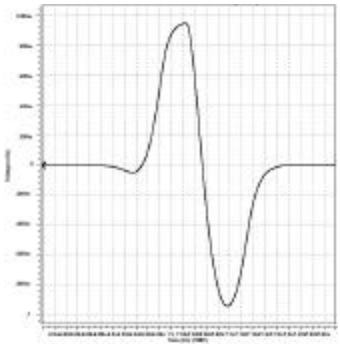


Figure 7: Timing Diagram of Power Saving Scheme

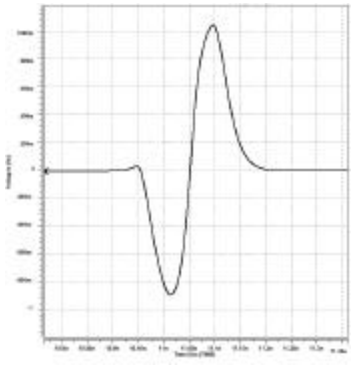
As shown in Figure 7, when the pulse generator is turned on and off, it generates small spurious pulses. Our simulation indicates that the spectrum of these pulses is out-of-band and will be filtered out by the bandpass filter that follows the pulse generator. The entire power saving scheme described above can be implemented as part of the state machine.

IV. Simulation Results

The proposed pulse generator was implemented for the TSMC 0.18 μm CMOS technology with a supply voltage of 1.8 volts. SPICE simulations were performed to examine the performance of the circuit, and Figure 8 shows Gaussian monocycle pulses generated by our pulse generator.



(a) Positive Gaussian mono-cycle



(b) Negative Gaussian mono-cycle

Figure 8: Gaussian Monocycle Pulses Generated

The generated monocycle pulses shown above have a peak-to-peak voltage of approximately 1.8 volts. Depending on the desired data rate and PRI, the output power can easily be increased or decreased by changing the size of the four transistors in the power amplifier.

V. Summary

We have presented a versatile low-power CMOS UWB pulse generator. Our simulation results show that our pulse generator can produce Gaussian monocycle pulses. This design can also be used as a rectified cosine generator in a multi-band system. We also presented a low-power design scheme such applications as RFID, which reduces the average power dissipation significantly. We are currently investigating other schemes to further reduce the power consumption at higher data rates.

All of the components except the RF choke can be implemented on a single CMOS chip, while the RF choke needs to be off-chip. We believe that as technology progresses and the speed of CMOS circuits increases, this type of pulse generator will become even more practical.

References:

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